

REMARKS

Summary Of Office Action

Claims 1-33 are pending in the above-identified application.

The Examiner has rejected claims 1-3, 16 and 17 under 35 U.S.C. § 102(e) as being anticipated by Kliever et al. U.S. Patent 6,781,889. Claims 4-15 and 18-33 have been allowed.

Summary Of Applicant's Reply

Applicant notes with appreciation the allowance of claims 4-15 and 18-33. Applicant has amended claim 16 to more particularly define the claimed invention. The Examiner's rejection is respectfully traversed.

Applicant's Reply to the Rejection of Claims 1-3, 16 and 17

Claims 1-3, 16 and 17 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Kliever. The Examiner's rejection is respectfully traversed.

Applicant's invention, as defined by independent claims 1, 16 and 17, relates to methods of deactivating at least one word line in a memory circuit. These claims define, generally, activating a plurality of word lines and deactivating at least one of that plurality of word lines, where the deactivated plurality of word lines constitute less than all of the activated word lines. For instance, claim 1 defines activating a plurality of word lines and deactivating one of the word lines, with the other word lines remaining active. Claim 16 defines activating a plurality of word lines and deactivating a subplurality of the word lines, the subplurality consisting of less than all of the activated plurality of word lines. Finally, claim 17 defines activating

a plurality of word lines and deactivating only one word line corresponding to a received address signal. These features are illustrated in applicant's specification, which states, for instance, in connection with FIG. 6:

[T]he ACTIVE signal is pulsed three times in transitions 603-605 to activate all three WLs. Advantageously, however, the WLs can each be deactivated without asserting the PRE-CHARGE signal, and the deactivation of each WL need not be simultaneous with the deactivation of other WLs. Rather, the three successive pulses of the ACTIVE signal shown in transitions 606a, 607a, and 608a deactivate the three WLs in turn, illustrated in transitions 606b, 607b, and 608b. Page 7, lines 11-20.

In contrast, Kliewer relates to a test mode of a semiconductor memory. Word lines in a memory can all be activated at the same time. In addition, all the even word lines of the memory can be activated at once, as can all the odd word lines. Kliewer explains:

A control signal CTRLX indicates to the word line decoder 22 that only a selection of word lines is to be activated. By way of example, only every second word line is activated in a first phase of the control signal CTRLX. By way of example, the word line 16 is activated, while the word line 17 remains inactive Afterward, in a second phase, the word line 16 is deactivated, and the word line 17 is activated The word line decoder is designed in such a way that it can activate the group of even word lines and the group of odd word lines separately from each other. Col. 5, line 65 to col. 6, line 25.

Thus, Kliewer shows a "strip-type" scheme that activates all the even word lines in a memory in a first phase, and activates all the odd word lines in a second phase. At the end of the first phase and prior to the second phase, all the even word lines are deactivated. Nowhere does Kliewer show or suggest the deactivation of at least one word line, where that

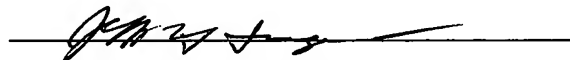
at least one word line is less than all of the word lines that have been activated, as defined in applicant's independent claims 1, 16 and 17.

For at least the reasons set forth above, applicant respectfully submits that independent claims 1, 16 and 17 are patentable. Accordingly, dependent claims 2 and 3 are also patentable. Applicant respectfully requests that the rejection to claims 1-3, 16 and 17 be withdrawn.

Conclusion

The foregoing demonstrates that claims 1-33 are allowable. This application is therefore in condition for allowance. Accordingly, reconsideration and allowance are respectfully requested.

Respectfully submitted,



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